AMBER model 5500

PROGRAMMABLE AUDIO MEASUREMENT SYSTEM

OWNER'S MANUAL

SECTION 5

THEORY of OPERATION

Issue 07 January 1989

THEORY OF OPERATION

5.0.0 INTRODUCTION

This section describes the various circuits used in the 5500 as a guide to circuit operation and to assist in troubleshooting. Reference should be made to Section 8, Schematic Diagrams. The second digit of each subsection in this Theory of Operation identifies the schematic being described. For example, Subsection 5.4, Detectors, describes Schematic 4.

Additional relevant details are provided in Section 6, Maintenance and Calibration and Section 7, Parts List.

5.1.0 FILTER & NOTCH (Schematic 1a, 1b)

5.1.1 GENERAL DESCRIPTION

This circuit forms a programmable notch filter used for fundamental rejection in the THD mode of operation. Additionally provided are High Pass, Band Pass, and Low Pass outputs for selective, narrow band or noise measurements. Constructed on a plug-in circuit board labelled (1) FILTER, it follows the PROMAG™ format.

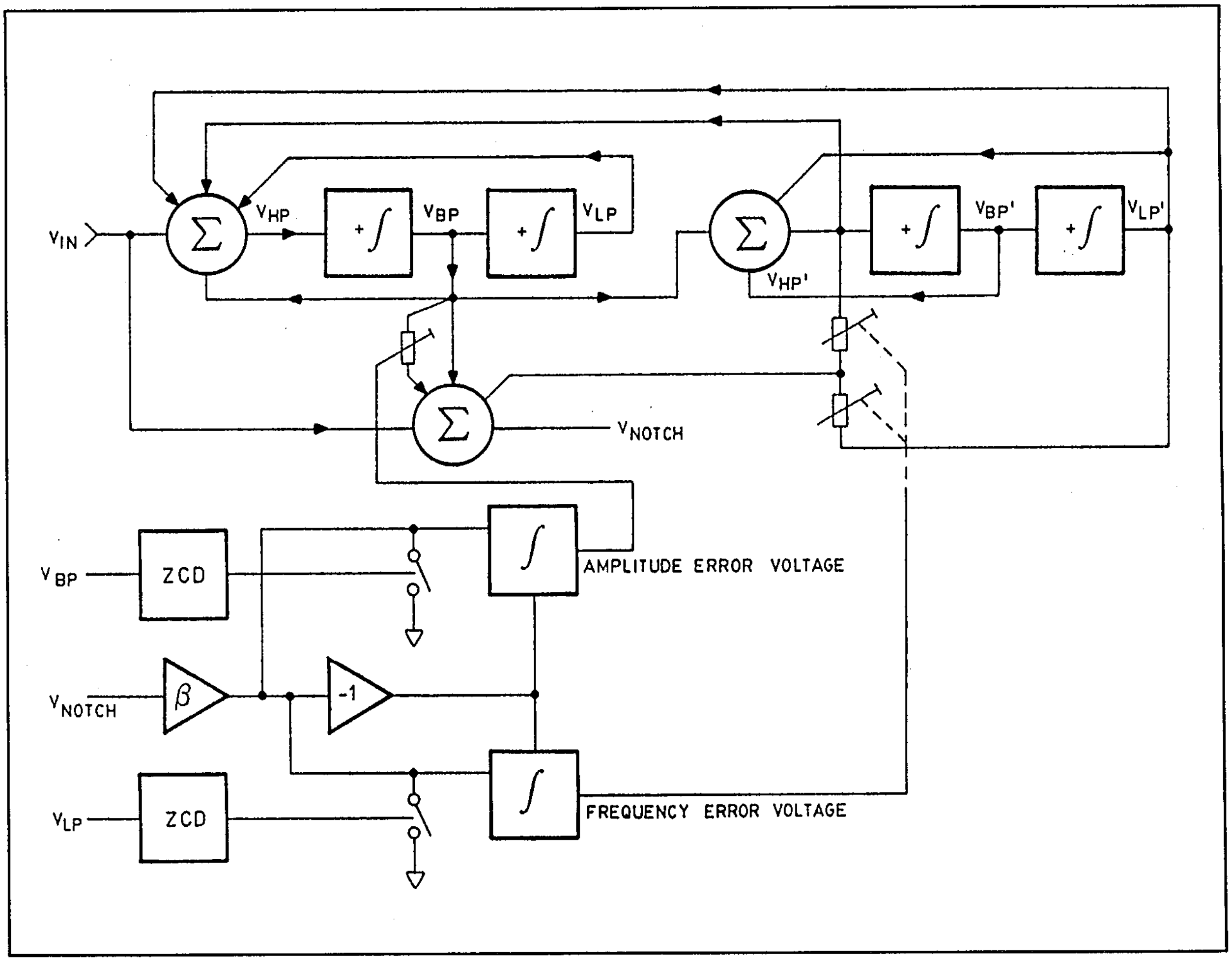
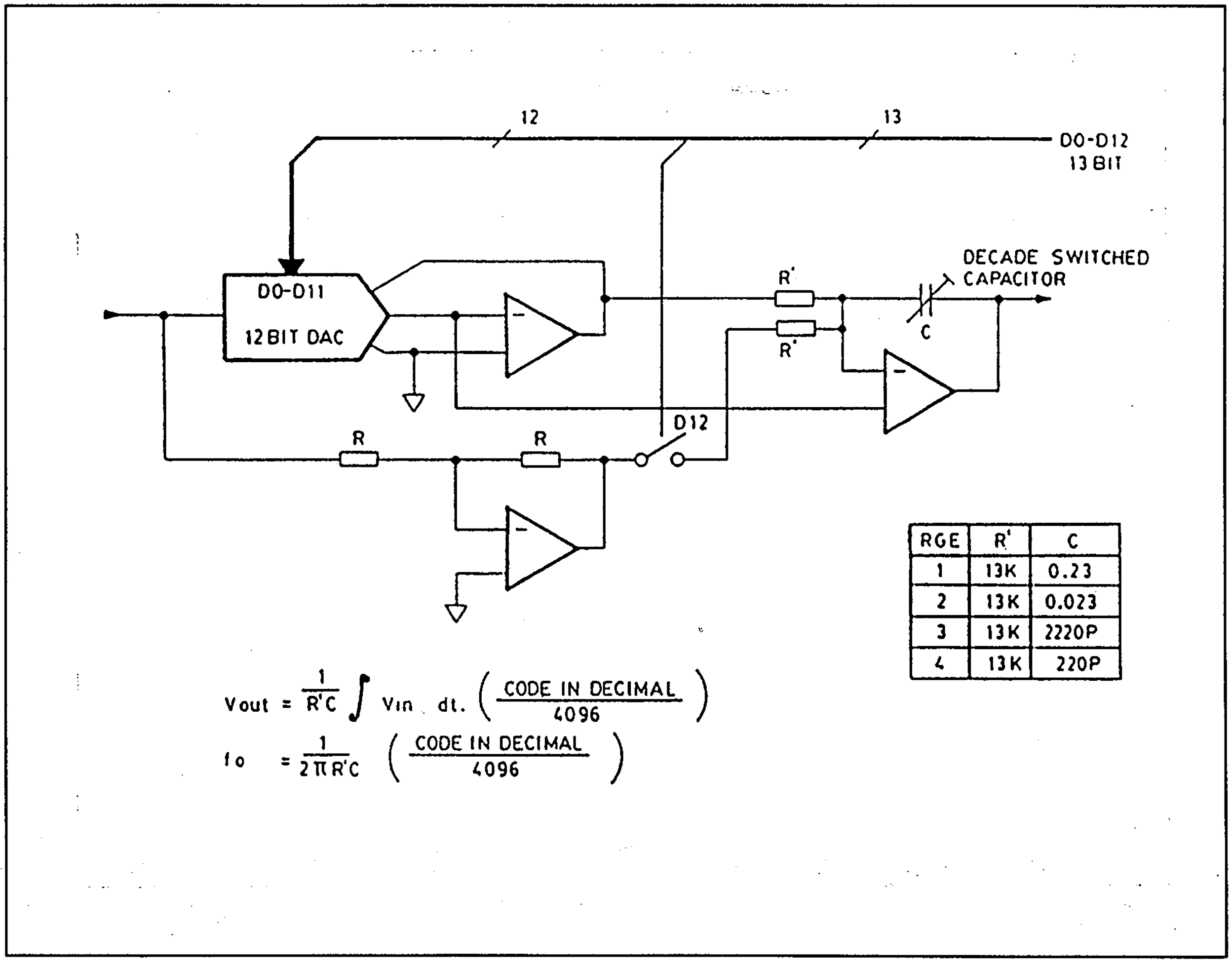


Fig. 5.1.2 Notch Filter & Servo

5.1.2 NOTCH FILTER

The notch filter is used to remove fundamental frequency in the THD measurement mode. It is variable from 10 Hz to 100 kHz. The filter also provides six additional outputs for narrow band measurements: four band pass modes with switchable "Q", one high pass output and one low pass output.

The main state variable loop consists of two coupled 2nd order state variable filters, each containing two non-inverting integrators and a differential summing amplifier. In the THD mode, an internal servo is enabled to auto-null the notch filter by an appropriate amount of phase and amplitude error correction.



RGE	R'	C
1	13K	0.23
2	13K	0.023
3	13K	2220P
4	13K	220P

$$V_{out} = \frac{1}{R'C} \int V_{in}\, dt \left(\frac{\text{CODE IN DECIMAL}}{4096} \right)$$

$$f_o = \frac{1}{2\pi R'C} \left(\frac{\text{CODE IN DECIMAL}}{4096} \right)$$

Fig. 5.1.3
Non-inverting integrator with feed forward compensation

5.1.3 FILTER INTEGRATORS

Center frequency of the notch filter is changed by relay switching four decade spaced capacitors in each respective integrator. A 13-bit multiplying DAC (Digital-to-Analog converter) is used to change the effective value of the integrator resistor providing fine frequency tuning within each decade. The 13-bit DAC is the combination of a monolithic 12-bit DAC plus a discrete 13th bit switched as the most significant bit. This 13th bit is used to reduce the effective noise gain of the integrator as frequency is switched towards the lower portion of a decade range.

Phase shifts in the cascaded amplifiers making up this integrator can cause undesirable "Q" enhancements at high filter frequencies. To counter this, a feed forward path is used to the Miller integrator to achieve a 3-fold increase in "Q" factor compared to an uncompensated integrator. This results in the total phase shift being equal to a simple Miller integrator alone.

5.1.4 NOTCH AMP AND SERVO

Notch or fundamental rejection is achieved by the summation of the filter input signal with the phase inverted Band Pass output of a State Variable Filter. At resonance, the band pass output of this filter will be exactly 180° out-of-phase with the input and thereby achieve fundamental rejection.

Due to component tolerances in the state variable loop, fundamental rejection of the notch filter alone is typically only about 40 dB, while over 100 dB is desired. To achieve this, a notch servo circuit is used to automatically trim the phase and gain to produce complete rejection.

The notch amplifier (U1021) output is amplified 40 dB by a residual gain amplifier, U1016A and U1016B. This signal is chopped at a rate synchronous with the fundamental signal by switches Q1004 and Q1005 such that the presence of fundamental in the signal will produce a non-zero average value at the output of the switch. Both normal and quadrature switches are used to accommodate any phase angle of error signal.

The frequency (or phase) servo correction circuit uses the filter low pass output to generate the chopping signal. The integrator following the chopper smooths the signal and produces a DC error voltage proportional to the amount of fundamental present in the signal. The integrator gain is also switched with frequency to optimize loop gain and decrease settling time at low frequencies. Capacitors are switched in four one decade steps from 10 Hz to 100 kHz.

The derived DC error voltage is used for phase correction of the filter loop by injecting some lead/lag quadrature phase signal to the notch amp.

5.1.5 FILTER AMPLITUDE SERVO

The same amplified residual error signal used in the previously described phase servo is fed to another chopper switch controlled by a square wave representing phase 2 (band pass output) of the state variable filter. At the amplitude servo, an equivalent full wave rectified error signal is presented to an integrator by summing the chopped signal and the inverse distortion signal. Thus any fundamental component synchronous with V_{BP} will create an error DC voltage at the integrator output. This error voltage represents the amplitude imbalance between V_{IN} and V_{BP} and is used to control an amplitude LDR (light dependent resistor - LED), Q1010, adjusting the amount of V_{BP} amplitude required for total cancellation.

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THEORY OF OPERATION

5.2.0 LOW DISTORTION STATE VARIABLE OSCILLATOR (Schematic 2a, 2b)

5.2.1 GENERAL DESCRIPTION

The oscillator is used as a primary signal source to generate low distortion sine waves, with four decades of frequency span from 10 Hz to 100 kHz. It also contains a square wave generator derived from the sine output. The oscillator may also be switched to a filter mode providing a second order low pass and band pass outputs with Q = 1.0. The oscillator consists of two non-inverting integrators and differential summing amplifier connected in a loop. An analog multiplier provides a variable level alternate feedback path around the summing amplifier for level control and is referred to as the AGC circuit.

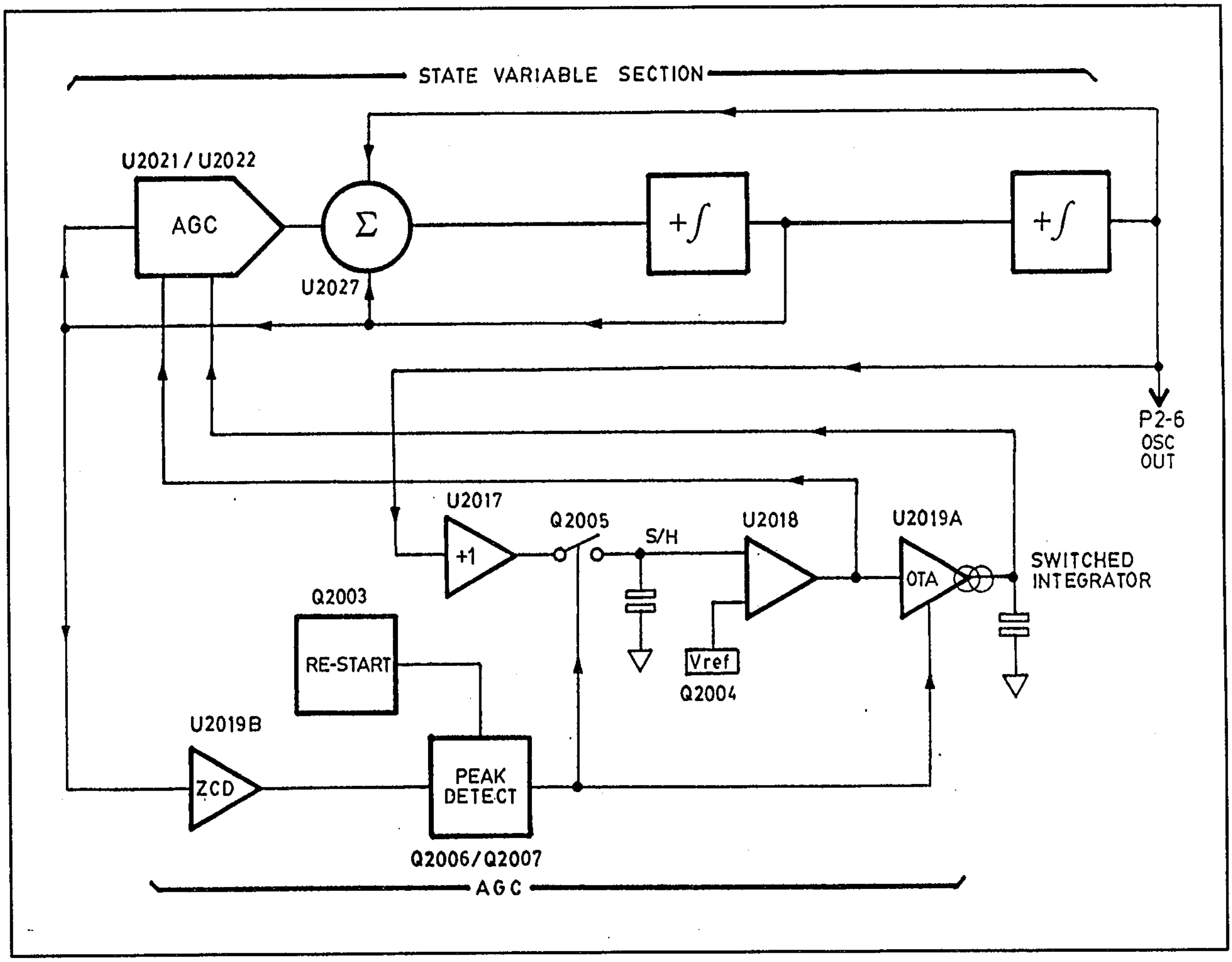
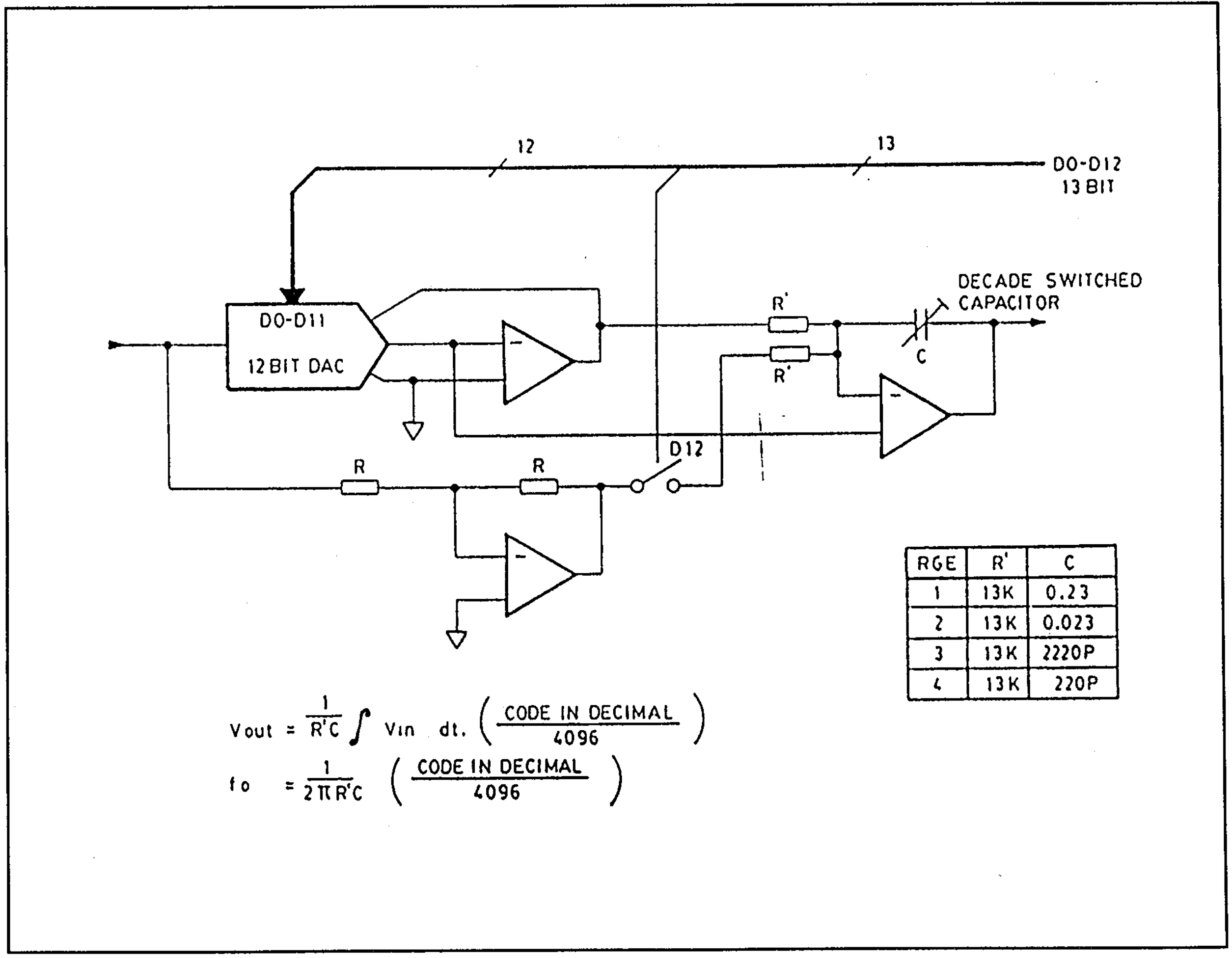


Fig. 5.2.1 Oscillator & AGC circuits simplified

5.2.2 INTEGRATOR

The oscillator frequency is changed by relay switching four decade spaced capacitors across the integrator and a 13-bit CMOS multiplying DAC is used to change the effective value of the integrator resistor providing the fine frequency resolution within each decade of frequency. The 13-bit DAC is the combination of a monolithic 12-bit DAC plus a discrete 13th bit switched as the most significant bit. This 13th bit is used to reduce the effective noise gain of the integrator as the frequency is switched towards the lower portion within the decade range.

Phase shifts in the cascading amplifiers making up this integrator can cause undesirable "Q" enhancements at high filter frequencies. To counter this, a feed forward path is used to the Miller integrator to achieve a 3-fold increase in "Q" factor compared to an uncompensated integrator. This results in a total phase shift being equal to a simple Miller integrator alone.



RGE	R'	C
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$$V_{out} = \frac{1}{R'C}\int V_{in}\,dt.\left(\frac{\text{CODE IN DECIMAL}}{4096}\right)$$

$$f_o = \frac{1}{2\pi R'C}\left(\frac{\text{CODE IN DECIMAL}}{4096}\right)$$

Fig. 5.2.2
Non-inverting integrator with feed forward compensation

5.2.3 OSCILLATOR AGC LOOP

The purpose of the AGC loop is to measure the oscillator output amplitude, compare it to a reference voltage corresponding to the desired level and generate an error voltage which when delivered to the multiplier, forces the oscillator output amplitude to equal the desired level.

A sample and hold circuit is used to measure the oscillator output level by driving the FET Q2005 on at each peak of the sine wave over a 13 μs window. The potential at the hold capacitor is compared with a reference voltage (V-Ref) and outputs an error voltage cycle by cycle. This error voltage is converted to a control voltage by a switched integrator whose gain is proportional to frequency. This control voltage is then used to drive the multiplier completing the loop. In the oscillator mode, the multiplier is used to supply a controlled amount of positive feedback to counter the damping resistor R2077. In the filter mode, the multiplier is disconnected from the filter loop and filter "Q" is set at 1.

5.2.4 SQUARE WAVE OUTPUT

Either sine wave or square wave outputs can be switched to output bus. The square wave generator is disabled when sine wave is selected to avoid the switching noise that would otherwise be generated. The sine wave output is used to feed a zero crossing detector "squaring" the output to a peak-to-peak voltage of approximately ±V Ref (+3.1623 V) supplied through P1-36. This squared-up voltage then drives a CMOS inverter as a buffer and swings the output within millivolts of V-Ref. This is then followed by an inverting op-amp to control the slew rate of the square wave so that succeeding stages are not over-driven.

Both duty cycle and gain trims are provided for calibration of the square wave.

A separate utility square wave output is provided on P1-10 for frequency measurement; this output is TTL compatible.

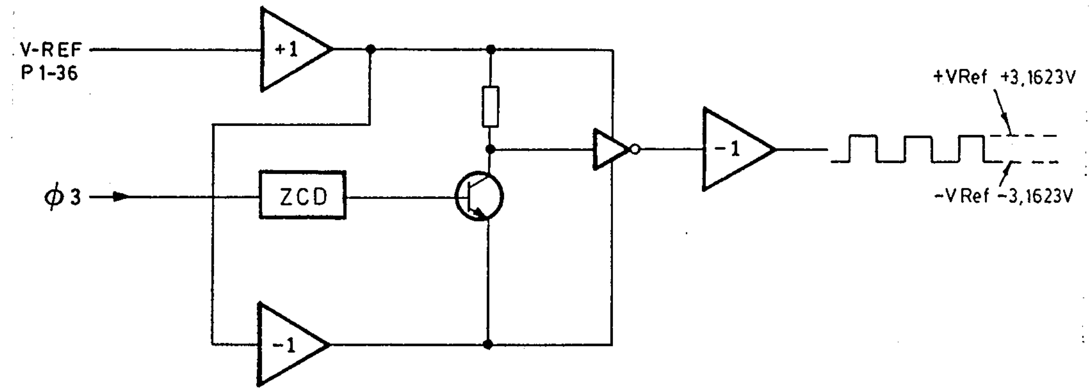

Fig. 5.2.4 Square wave generator

5.3.0 INPUT ATTENUATOR & PREAMPLIFIER

5.3.1 GENERAL DESCRIPTION

This circuit serves to normalize signal levels presented to the INPUT of the 5500 system. Also referred to as PGA (Programmable Gain A), it is constructed on a plug-in PROMAG™ circuit board labelled (3) PREAMP. Its circuit appears on Schematic 3a, 3b.

5.3.2 INPUT TERMINATION

Two input resistors are provided for switchable input termination, 150 ohm and 600 ohm, 2 Watt for both A and B inputs. Termination is not provided for internal oscillator receive. These resistors switch across high and low inputs of a balanced input and across high and ground of an unbalanced input. They are selectable by a front panel control or GPIB command.

5.3.3 INPUT COUPLING CAPACITORS

Input signal is AC coupled via two 1 μf, 400 Volt film capacitors. These are matched to within 0.5% to achieve good low frequency CMRR.

5.3.4 INPUT ATTENUATOR

Following the AC coupling, the signal then appears across two 100 k ohm input attenuators used to normalize high input signal levels to +10 dBV. These are relay switched in 10 dB steps giving attenuations of 0 dB, -10 dB, -20 dB and -30dB. Input compensation capacitors are used to counter stray capacitances which would effect high frequency response.

5.3.5 PROTECTION

At -10, -20 and -30 attenuation settings, input circuitry is protected by the current limiting of the attenuator resistors. However, when set to unity gain and suddenly presented with a high voltage, further input protection is necessary until auto-ranging attenuates the signal to a safe level. Under these overload conditions a light bulb, which has a cold resistance of approximately 600 ohms, will illuminate presenting a high impedance and serve as a current limiter. A 0.01 μf capacitor is connected across the light bulb to compensate for its inductance. Referring to Figure 5-3, diodes D1 through D6 complete the protection circuit.

5.3.6 CASCODE PREAMP

Two hybrid preamps are used for front-end gain. A cascode configuration is used for low input capacitance and wide bandwidth. The FETs used are biased at 2 mA each by an active current source. Cascode clamp limits V_{DG} to less than 2 diode drops for all voltage excursion levels and removes the effect of C_{GD} (Miller capacitance) increasing the bandwidth of the input stage. This coupled with its active drain load has ample current to charge C_c of the following operational amplifier, raising the dominant pole of the composite operational amplifier. The operational amplifiers, U3005 and U3012, are unity gain stable. As they have a slow input stage, it is shutdown by tying pins 2 and 3 to ground and replaced by the FET cascode stage. Some over-compensation is used (C3016, C3042) to ensure stability.

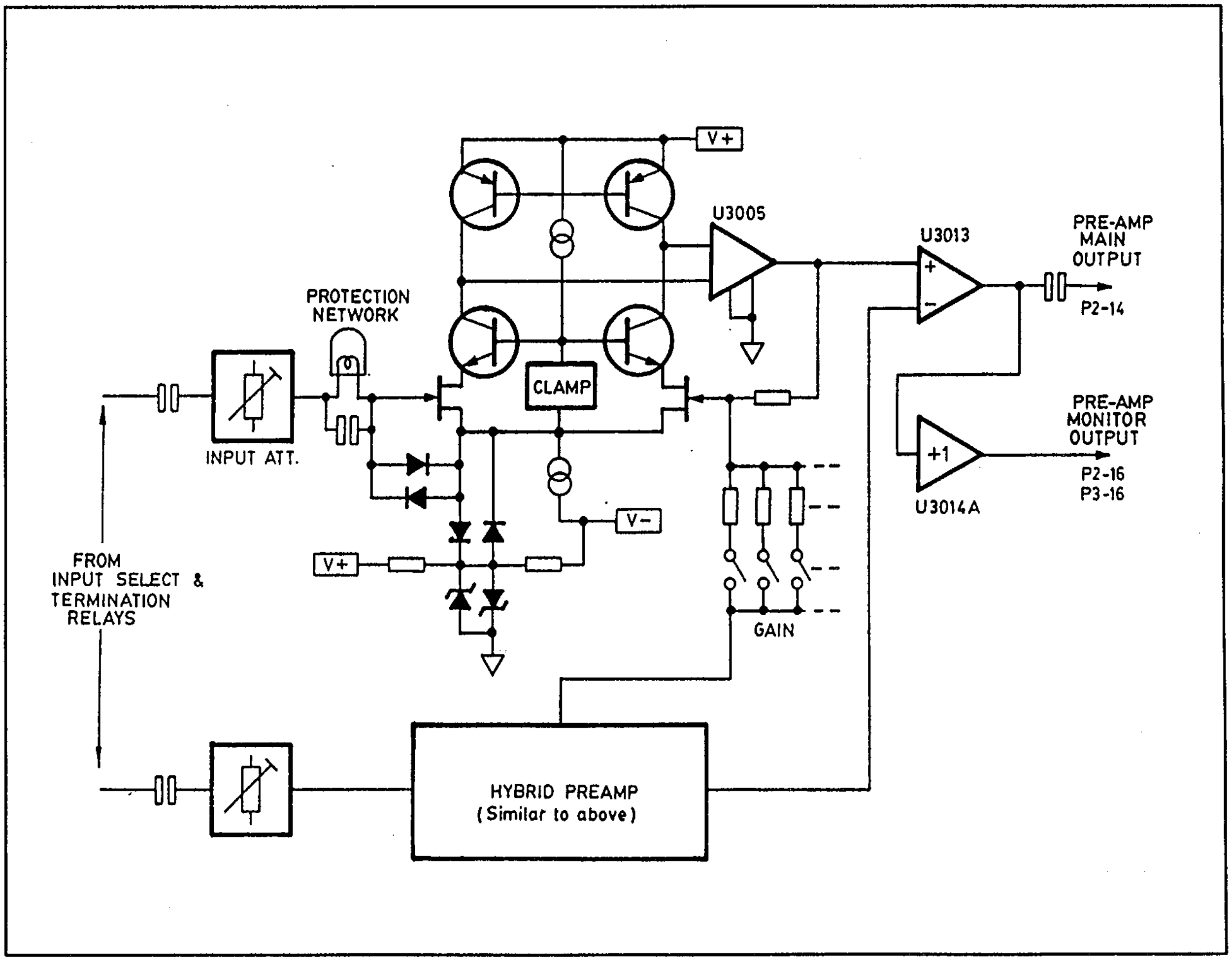

Fig. 5.3 Programmable Gain A simplified

5.3.7 OUTPUT DIFFERENTIAL AMPLIFIER

Outputs of the cascode preamps are combined through a classic differential amplifier (U3013) coupled with a DC feedback integrator (U3014B) to null out DC offsets. Broad band and high frequency common mode rejection trims are provided at this stage followed by a unity gain buffer (U3014A) to provide a monitor output for general utility use.

Table 5-3 Preamp Gain/loss

LEVEL MODE			DISTORTION MODE		
NOMINAL INPUT SIGNAL RANGE dBV	ATTENUATOR LOSS dB	PREAMP GAIN dB	NOMINAL INPUT SIGNAL RANGE dBV	ATTENUATOR LOSS dB	PREAMP GAIN dB
+40 to +30	-30	0	+40 to +35	-30	0
+30 to +20	-20	0	+35 to +30	-30	+5
+20 to +10	-10	0	+30 to +25	-20	0
+10 to 0	0	0	+25 to +20	-20	+5
0 to -10	0	+10	+20 to +15	-10	0
-10 to -20	0	+20	+15 to +10	-10	+5
-20 to -30	0	+30	+10 to +5	0	0
			+5 to 0	0	+5
			0 to -5	0	+10
			-5 to -10	0	+15
			-10 to -15	0	+20
			-15 to -20	0	+25

NOTE: 1) Auto-ranging hysteresis will cause a variation of approximately +0, -2 dB of nominal input range level.

2) Gains and attenuations are set by 0.1% tolerance resistors achieving a gain/loss accuracy of 0.01 dB.

5.3.8 CONTROL LOGIC

The preamp board analog circuitry is controlled by the host CPU through the digital interface resident on the board. The circuit design follows the PROMAG™ Digital Interface standards. Address and data descriptions are in hexadecimal notation.

5.3.9 DECODING LOGIC

With reference to schematic #3, address decoding is by U3011 (74LS85, 4-bit magnitude comparator) and U3010 (74LS138, 1-to-8 decoder). Using the decoding links CL0, CL1, CL2, and CL3, U3011 decodes the address block between 80 and 87 inclusive. This then qualifies U3010 where, when in a write cycle, only address 80 and 81 are used to control all functions on the preamp board. The data bus is routed to U3006 (74LS273, octal D flip-flop) and in reduced form, i.e. D0 - D5, to U3016 (74LS174, hex D flip-flop). Both flip-flops have their master reset inputs connected to the QUIET STATIC BUS reset line so that on power-up the flip-flops are set to logic low outputs. Data is latched into U3006 at address 80 and into U3016 at address 81.

5.3.10 FUNCTIONAL & GAIN CONTROL

The preamp functions are controlled by individual or groups of data bits through three ULN2003 transistor arrays (U3015, U3004, U3008). Four functional groups are implemented by the interface design. U3003 (74LS259) decodes three data bits to control the positive gain relays. U3007 decodes two bits for controlling the attenuator relays. And U3009 decodes two bits for input selection control. The input termination select control is by two data bits latched by U3016.

5.4.0 DETECTOR BOARD (Schematics 4a, 4b)

The analog circuitry of the detector board selects various AC signal sources from the 5500, conditions them and, through digitally controlled switching circuits under CPU control, sends two signals to the CPU for amplitude and frequency readings respectively. Both signals are logic level pulses whose frequencies have a direct relationship to the amplitude and frequency of the corresponding analyzer signals. The CPU, by selecting the sources for these two signals, determines all automated system settings and operations.

5.4.1 PGC (PROGRAMMABLE GAIN "C")

The PGB and weighting filter output is fed on P2-48 to a FET buffered operational amplifier with a high input impedance and low bias current (Q4003 and U4020). The input signal is DC coupled through a 2k2Ω resistor. The FETs are biased at 5 mA by an active current source (Q4004 and Q4005) and feed the second stage of a 5534 (U4020) with its front end shut down. One of three gains is selected by a DG211 CMOS analog switch (U4021) under control of the CPU through the interface logic. The PGC stage gains are 0, +10, and +20 dB and its output is buffered by half of a LF412 operational amplifier (U4005).

The PGC output is fed to various circuits on the detector board. PGC is buffered by half of a TL072 (U4017) and is connected to the MEASURED FUNCTION MONITOR BNC on the front panel. The output is protected by a series resistance and zener diode clamps. PGC also feeds P1-34.

5.4.2 RMS CONVERTER

PGC is also fed to an AD536A rms-to-DC converter IC (U4009). This device computes the true rms value of a complex input waveform. Using a CPU controlled method of changing the effective value of the external capacitor, which sets the averaging time constant, a performance balance is achieved between output ripple and settling time. A 4053 CMOS switch (U4010) adds capacitance to the fixed capacitor C4032 to optimize performance. Output ripple is further reduced by a single pole post filter (C4033). An internal buffer amp provides the rms output to one input of the level multiplexer.

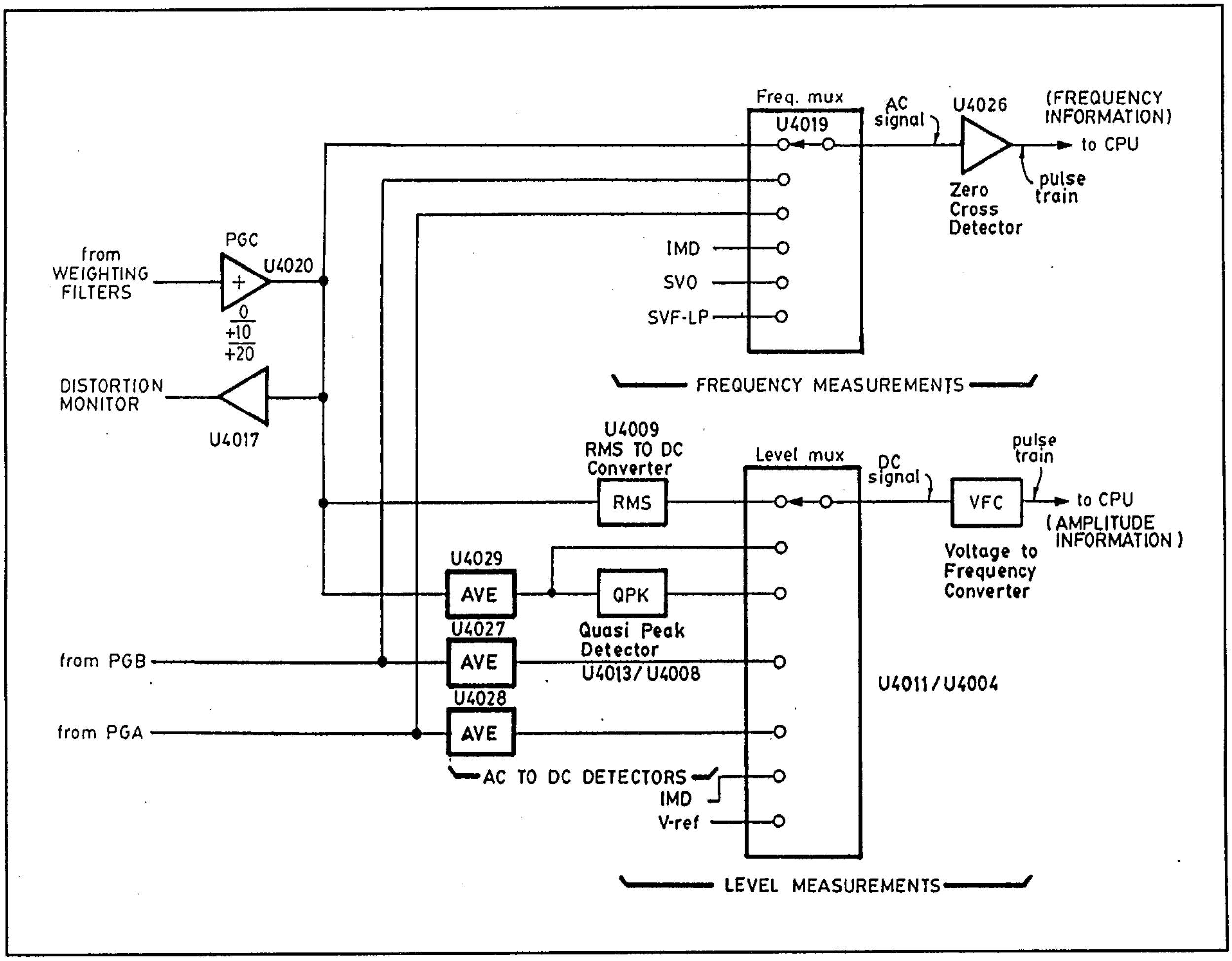

Fig. 5.4 Detectors and switching simplified

5.4.3 ABSOLUTE VALUE AVERAGING

PGC is additionally fed to a precision absolute value circuit (U4029) used as an average response detector for level measurement. Gain matching to the rms detector is provided by the software AUTOCAL routines.

5.4.4 LEVEL DETECTION

The host CPU selects, by means of U4004 (DG508, CMOS analog multiplexer), the source signal for amplitude detection. All sources to the level multiplexer are normalized and the output is buffered by U4007. Zener diode clamps on the input prevent extreme out-of-range conditions at later stages. The output of the buffer goes to a DG211 switch (U4003) where the CPU can select the output or one reduced by 6 dB. This is now further buffered by the second half of U4007 (TL072). The buffer output is sent to P1-38 and to the input of the voltage-to-frequency converter (U4006 - VFC 32). With the input and offset trims (VR4002 & VR4001), the voltage-to-frequency converter is calibrated so that a normalized signal will be between 0 V and 3.162 V producing a "within range" frequency output. This is a pulse train and, by referencing this against a master clock, the CPU is able to determine the represented amplitudes.

As stated previously, the host CPU selects the source to the voltage- to-frequency converter by the eight channel multiplexer, U4004. In normal operation, the CPU scans different points in the 5500 system to maintain gain stages at their proper settings.

5.4.5 QUASI-PEAK DETECTOR

The third source to the multiplexer is the Quasi-peak detector which meets CCIR 468-3 specifications for attack/decay time constants.

The output of the average detector is tapped at U4029, pin 7 and brought through a trimmable voltage divider for level matching. U4013B is an absolute value buffer. The input and output RC networks around U4013A provide specific charge/discharge time constants. The circuit formed by U4008, Q4002 and associated components form the peak hold with preset decay circuit. This output is fed to the level multiplexer.

5.4.6 PGA-PGB DETECTORS

Gains are monitored and set by the host CPU, by use of average responding amplitude detectors, whose inputs are from the preamp and PGB board respectively. The detectors are identical to the average detector for PGC. They are formed by U4028 and U4027 and feed the next two inputs to the level multiplexer.

5.4.7 IMD DETECTOR
(Requires option 002)

Input to the level multiplexer is via P2-42. An average detector on the IMD PROMAG™ board provides the normalized DC level send to the detector board. A simple RC network formed by a low pass single pole filter provides signal conditioning at the multiplexer input. When the IMD option is installed, the CPU monitors distortion reference levels through this detector.

5.4.8 V-REF

V-REF is a precision voltage source of 3.162 V generated by Q4001 (TL431, precision voltage regulator) and buffered by U4005A. This is fed to the last input of the level multiplexer, to the P1 bus and as bias to the summing node of the VFC32. It is also fed through a switch in the DG211 (U4003) to the summing node of U4005B (PGC input buffer) as a method of controller calibration.

5.4.9 FREQUENCY DETECTOR

PGC, PGB, and PGA are also fed, while they are normalized bipolar waveforms, to the frequency multiplexer formed by a DG508 (U4019). This multiplexer's output is AC coupled to a TL311 (U4026) high speed comparator to produce a square wave representing the signal frequency which is fed to the CPU. The remaining five inputs of the frequency multiplexer are assigned to the P2 and P3 bus. Certain inputs have been assigned to the IMD option to read recovered LF and HF and to the internal oscillator to read generator frequency directly.

5.4.10 LOGIC CIRCUITS

The logic circuitry on the detector board is divided into two sections. The QUIET STATIC BUS LOGIC provides an additional set of bus transceivers for address, data, and control signals buffering to other PROMAG™ modules (which only become active when the PROMAG™ modules are accessed). This in effect keeps the activity on the P1 bus on the motherboard to a minimum to reduce the possibility of polluting any analyzer functions or measurements. The second section is the digital interface to the detector board functions. All addresses and data are in hexadecimal notation.

5.4.11 STATIC BUS INTERFACE

With reference to Schematic #4b, the STATIC BUS buffers of the CPU connect to the detector board on J4002 by a 50-wire ribbon cable. The QUIET STATIC BUS interface logic forms the CPU signal buffering to the 5500 system P1 bus. All PROMAG™ module's logic interface is via the motherboard P1 bus. The STATIC BUS address lines are 8 bits which sets STATIC BUS I/O to a 256 byte address block.

The address lines buffer (U4015) is enabled by any STATIC BUS address between 80 and FF because A7, through inverter U4018, is used to enable U4015. Pull-up resistors for A0 - A6 and R/W keep the QUIET STATIC BUS in a non-floating mode when not accessed. Address line A7 on the QUIET STATIC BUS is continually a logic high by being connected only to a pull-up.

In a write cycle to the QUIET STATIC BUS, the R/W line will set the direction of the data bus transceiver U4022. The logic low of the R/W line also, through gate U4025 and U4018, immediately enables U4022. A7 being high on the STATIC BUS also qualifies the EN* signal to be sent through to the QUIET STATIC BUS by gate U4025. Pull-ups are also used on the data bus and EN* signal to keep them in a non-floating state when not accessed.

In a read cycle, the R/W line again sets the direction of the data bus driver but the driver will only be enabled when EN* is true thus preventing erroneous data from being on the data bus.

All other pins on J4002 (STATIC BUS) and P1 (QUIET STATIC BUS) are connected together 1-to-1.

5.4.12 DETECTOR INTERFACE

The detector board analog circuitry is controlled by the CPU through the digital interface resident on the board. The interface follows the PROMAG™ digital interface standards to hardware usage. Address decoding is by U4016 (74LS85, 4-bit magnitude comparator) and U4014 (74LS138, 1-of-8 decoder). Using links CL1 and CL3, U4016 decodes the address block of 28 to 2F. The first two addresses in this block are selected for use from U4014 (28 & 29) and only in write mode by using the R/W line as a qualifier.

Two 74LS273 octal D flip-flops are used to latch data from the CPU when either of them is addressed by tying their clock inputs to decoder outputs. U4024 is clocked by address 28 and U4023 by address 29. The MASTER RESET pins are connected to the system RESET* on the QUIET STATIC BUS to ensure known states whenever the instrument is powered up.

The latched outputs are used as individual bits or in groups as coded controls. The level and frequency multiplexers use binary codes and enable information from U4024 while the information in U4023 is further adapted to the hardware that is controlled. U4012 (DG508) is used as an active high 1-of-8 decoder with the high level being set to +15 V.

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5.5.0 POWER AMPLIFIER (Option 001)

5.5.1 GENERAL DESCRIPTION

This circuit, constructed on a plug-in PROMAG™ circuit board labelled (5) POWER AMP, serves to amplify the fixed level oscillator output and provides coarse (-20 dB steps) and fine attenuation for precision level setting. The circuit card occupies two PROMAG™ slots and contains a plug-in daughter board which is shielded within its own metal enclosure. The main circuit card follows the PROMAG™ board convention with its associated P1, P2 and P3 plug-in tongues. Attached to the metal shield box is a heat sink required for thermal dissipation of the output transistors. (Though heat sinking is provided, this board is not intended to operate in free air but requires the air currents generated within the 5500 frame to assist in thermal dissipation.) An isolation transformer is also attached to the shield box and is itself contained in a mumetal shield.

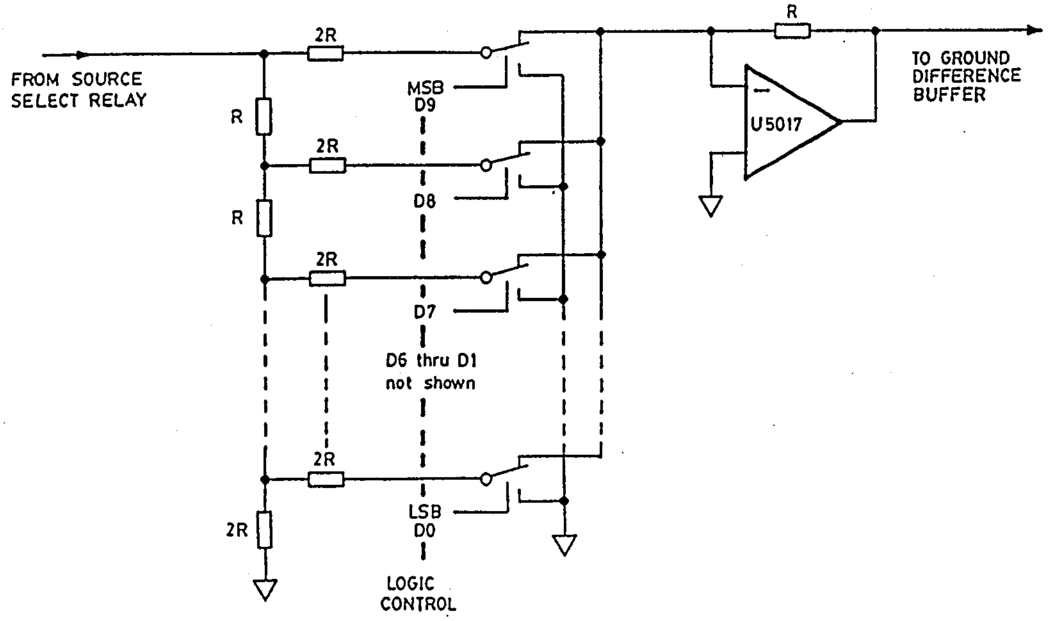

Fig. 5.5.1 10-BIT DAC, fine level control

5.5.2 10 BIT DAC FINE LEVEL CONTROL (Referring to Figure 5-5.1 and Schematic 5)

The main or auxiliary signal source bus is selectable with a relay to the input of a 10-bit discrete MDAC (multiplying digital to analog convertor). The R-2R resistor ladder is comprised of a combination of 10 k and 20 k R-nets and discrete resistors. The switches are 4053 "form C" CMOS switches. This allows the fine level control of 0.03 dB or better over a 10 dB range.

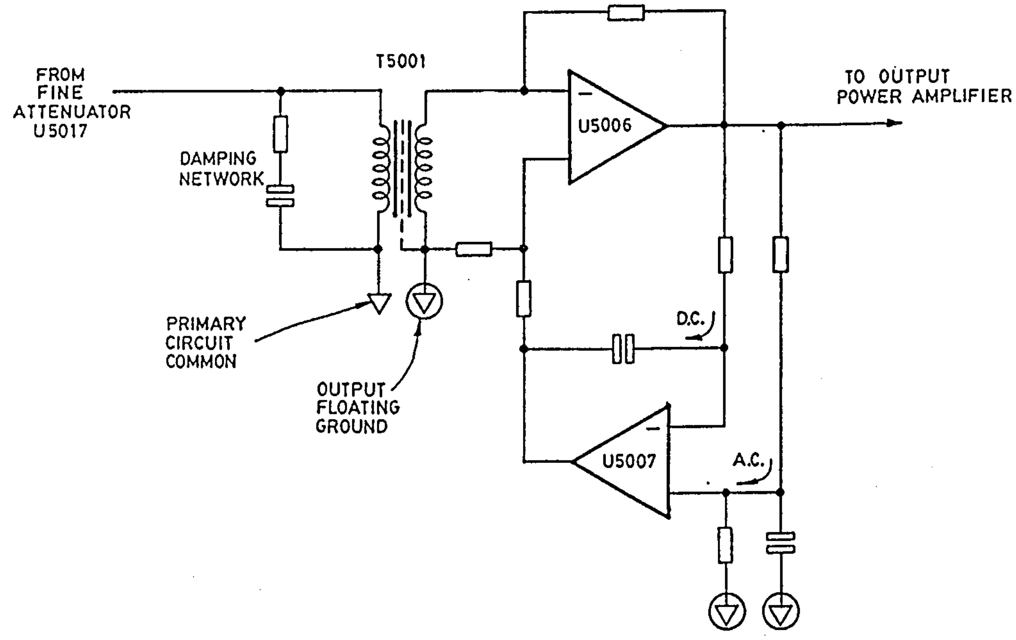

Fig. 5.5.2 Ground difference buffer

5.5.3 GROUND DIFFERENTIAL BUFFER (Figure 5-6)

A transformer is used to couple the ground referred input to the floating power amplifier (Figure 5-5.2). A combination of DC negative feedback and AC positive feedback provide linearization and DC stability to the negative impedance coupled transformer used in a current mode. The two primary and secondary windings are paralleled in a 1:1 transfer ratio. Since I1/I2 = N2/N1, the voltage gain of this stage is unity. Damping is provided at the primary winding for best square wave response. The low frequency distortion reduction is directly proportional to the positive feedback factor and set by R5004. This is chosen to cancel R_{sec} of the transformer. The floating buffer amplifiers are powered from bipolar 15 Volts derived from the ±35 Volt via discrete voltage regulators. (Q-5001, Q-5020)

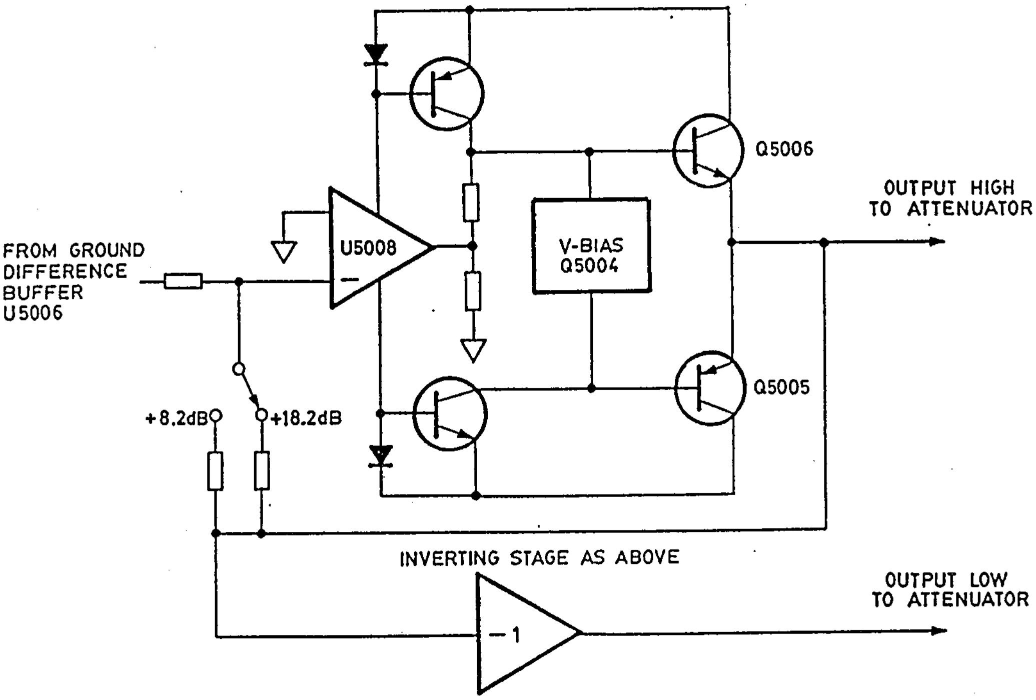

Fig. 5.5.3 Output power amplifier simplified

5.5.4 FLOATING POWER AMPLIFIERS (Figure 5-5.3)

Output from the transformer buffer is fed to an inverting power amplifier with switchable gains of 8.2 dB and 18.2 dB. This amplifies the oscillator output to the maximum 33 V rms (open circuit) required. The power amplifiers use a pair of zener diodes to limit voltage at ±15 Volts to U5008. Current through the upper and lower transdiode Q- 5013, Q-5015 is mirrored to the level shifters at unity current gain but large voltage gain with a V_{BE} multiplier connected at its mid- point. Interstage series voltage feedback is provided from this node to pin 6 of U5008. The bias transistor is thermally connected to the output transistors on the heat sink block to provide thermal feedback and prevent thermal runaway. The output transistors provide the necessary current gain to drive both A and B outputs loaded to full level at low distortion.

Current limiting is implemented by sensing current through output emitter resistors and clamping the output drive when the 200 mA threshold is exceeded. Output from the upper power amp is followed by an identical power amp but configured as a unity inverter to provide push/pull operation. ± 0.1% resistors are used where gains or attenuations are affected to preserve longitudinal balance (>60dB). Current mode operation is used to eliminate common mode distortion caused by the input stage when used in a non-inverting mode.

5.5.5 OUTPUT COARSE ATTENUATOR

A constant output impedance attenuator is used following the power amplifiers to provide attenuations in 20 dB steps from unity to -80 dB and an output impedance of 50 ohm. Switchable resistors are used in series to increase the source impedance proving 150 ohm and 600 ohm outputs. The top most resistors are high power type (2 Watts & 1 Watt) to sustain the maximum current if the outputs are shorted or driving an extremely low impedance.

Table 5-5 Power amp/attenuator gain chart

POWER AMPLIFIER GAIN	COARSE ATTENUATOR LOSS dB	BALANCED OUTPUT LEVEL (150 Ω source, 600 load) dBm	UNBALANCED OUTPUT LEVEL (open circuit) V rms
+18.2dB	0	+32dBm	16.5V
+8.2dB	0	+22dBm	5.22V
+18.2dB	-20	+12dBm	1.65V
+8.2dB	-20	+2dBm	522 mV
+18.2dB	-40	-8dBm	165 mV
+8.2dB	-40	-18dBm	51.2 mV
+18.2dB	-60	-28dBm	16.5 mV
+8.2dB	-60	-38dBm	5.12 mV
+18.2dB	-80	-48dBm	1.65 mV
+8.2dB	-80	-58dBm	512 μV

5.5.6 OUTPUT IMPEDANCE SWITCHING

A 50 ohm impedance attenuator is used for each power amplifier. The front panel BNC unbalanced output is available, with a 50 ohm source impedance, from the upper power amplifier. In the balanced mode, 150 ohm and 600 ohm source impedances are available. These impedances are achieved by the addition of 25 ohm resistors in series for 150 source and 250 ohm resistors in series for the 600 ohm source.

A zero source impedance power amp output is routed through P3 to drive the optional B output attenuator. The attenuator output is also relay switched as a send signal to the analyzer INPUT for internal level check.

5.5.7 GROUND/FLOAT SWITCHING

Power amp floating common and analog signal common are not electrically connected in the FLOAT mode.

In the relay switched GROUND mode, analyzer and oscillator commons are connected through a light bulb F-5001 which exhibits a cold DC resistance of approximately 500 ohm. Its inductive reactance is countered with a shunt capacitor of 0.068 μf which results in an impedance of approximately 24 ohm at 100 kHz when in the ground mode.

5.5.8 CONTROL LOGIC

The power amp board's analog circuitry is controlled by the host CPU through the digital interface resident on the board. The circuit design follows the PROMAG™ digital interface standards. All information in this circuit description treats the power amp main board and daughter board as one since only analog considerations define the daughter board requirements. Addresses and data descriptions are in hexadecimal notation.

5.5.9 DECODING LOGIC

With reference to schematic #5, address decoding is by U5016 (74LS85, 4-bit magnitude comparator) and U5015 (74LS138, 1-of-8 decoder). Using the decoding links CL1, CL2, and CL3, U5016 decodes the address block of C0 to C7. This then qualifies U5015 where, when in a write cycle, address C0, C1 and C2 are used to control the power amp functions.

The data bus is routed to U5010 (74LS273, octal D flip-flop) and to U5011 and U5012 (74LS174, hex D flip-flop). U5011 and U5012 use a six bit data bus, D0 - D5. The master reset pin of each flip-flop is connected to the QUIET STATIC BUS reset line so that all outputs are set logic low on power-up.

5.5.10 POWER AMP INTERFACE

U5012 and four bits of U5011 are used to latch data for the 10-bit DAC attenuator circuit. These are addressed at C2 and C1 respectively. The circuit requires 10k pull-up resistors to +7.5 V for the correct logic high level.

The remaining controls are relay drives. ULN2003, darlington transistor arrays (U5004 and U5005), are used as the drivers with the flip-flop outputs as controls. Data bit D4 and D5 from flip-flop U5011 control the GND/FLOAT relay and the input main/aux relay respectively; they are at address C1. Address C0 has the remaining controls defined as follows: one bit for the output enable relay, 3 bits for the output termination selection and 4 bits for the output attenuator control. Three of these 4 bits for output attenuator control are used in an encoded format and feed U5003 (74LS259) which is used as 1-of-8 logic high decoder.

5.6.0 IMD OSCILLATOR AND ANALYZER (Option 002) (Schematic 6a, 6b)

5.6.1 GENERAL DESCRIPTION

The IMD section, an option to the 5500 system, is constructed on a plug-in PROMAG™ circuit board labelled (6) IMD, containing both low frequency oscillator and IMD analyzer. It uses the normal system oscillator for high frequency generation and performs both popular IMD tests, SMPTE and CCIF. In the SMPTE mode, selectable mix ratio permits choice of 1:1, 2:1, 4:1, and 10:1 amplitude ratios. In the SMPTE mode, the HF signal may be between 3 kHz and 100 kHz while the LF component has a choice of one of eight frequencies between 40 Hz and 500 Hz. In the CCIF mode, difference frequency is selectable to be 1-of-8 choices and mean frequency can be 4 kHz to 100 kHz.

5.6.2 LOW FREQUENCY OSCILLATOR

This circuit is based on the state variable filter comprised of a summing amplifier (U-6013A) followed by two integrators in cascade (U- 6012). R6044 supplies positive feedback around the loop and an AGC circuit (U-6013B) controls the amount of negative feedback to just sustain oscillation. Full wave rectified current is compared with a reference current derived from a precision voltage reference, Q-6005. This is made variable to adjust the level of oscillation. The sum of both currents are fed to a summing integrator whose output is an error voltage used to drive a FET feedback control element, Q-6004. Drain- source resistance of the FET is dependent on the applied gate source error voltage, which will control the amount of feedback to sustain oscillation. Output is taken from the low pass integrator (U-6012B) which, through double integration, has the lowest harmonic distortion.

Frequency of oscillation is controlled by switch selection of both integrator resistors and follows the time constant of $F_O=1/2RC$. One of eight of the following frequencies is available: 40 Hz, 50 Hz, 60 Hz, 80 Hz, 100 Hz, 125 Hz, 250 Hz, 500 Hz.

5.6.3 SMPTE GENERATOR

SMPTE IM source has the following characteristics:

Low frequency limits are 40 Hz to 500 Hz
High frequency limits are 3 kHz to 100 kHz
Amplitude ratios are 1:1, 2:1, 4:1, 10:1, LF to HF

A mixing amplifier (U-6017) is used on the IMD board to select one of four amplitude mix ratios. The mixed output, regardless of ratio, has the same peak-to-peak amplitude as the equivalent THD mode oscillator sine wave.

5.6.4 CCIF GENERATOR

The CCIF generator produces a twin tone high frequency signal mixed at a 1:1 amplitude ratio whose difference frequency does not exceed 1 kHz and mean frequency is between 4 kHz and 100 kHz. This is achieved on the IMD board by a discrete balanced modulator using matched FET Q-6003 as variable resistive elements. The balanced modulator converts its two input signals to two new signals with frequencies equal to the sum and difference of the input signals. The internal 5500 oscillator is used as the modulation frequency and the IMD low frequency oscillator is used as the carrier frequency. Thus, the resulting composite signal will consist of a twin-tone signal whose mean frequency is the same as the HF oscillator and whose difference frequency is twice the LF oscillator (i.e., the "offset" frequency). A trim adjustment is provided for carrier suppression and another provided for gain calibration. This adjustment is made to obtain the same peak-to-peak output as the THD mode oscillator sine wave at P2-6. Output from the balanced modulator is fed to a 4-pole elliptical filter U-6007, U-6016 with a 500 Hz notch for further carrier suppression, and also provides additional gain for signal level normalization.

5.6.5 OUTPUT SELECT

Mode selection is via relay switching providing IMD on/off select and SMPTE/CCIF select. The balanced modulator for CCIF twin tone generation is switched off when not in the CCIF mode to prevent signal leak through and contamination of IM residual.

5.6.6. ANALYZER

SMPTE IMD

The composite input signal in the SMPTE distortion mode, which appears at preamp out, is presented to the input of the 8 pole, 2 kHz, High Pass Butterworth filter. This filter removes virtually all of the low frequency component leaving only the high frequency carrier with the IMD components. Depending on the composite input amplitude ratio, 1 of 4 succeeding gains will be selected to normalize the high frequency level.

GAIN	LF TO HF RATIO
0dB	1:1
+6dB	2:1
+12dB	4:1
+20dB	10:1

This normalized HF level is demodulated by an AM detector formed by a precision absolute value circuit. The output, which appears at P2-24, will be a detected version of the HF carrier signal used to ratio against the distortion signal for distortion level calculations. This output is then AC coupled into a 10 pole 1 kHz Butterworth 10 dB gain low pass filter whose AM product output is the intermodulation distortion.

5.6.7 CCIF IMD

When the instrument is switched to the CCIF IMD mode, the preamp output is connected directly to the 10 pole 1 kHz low pass filter with 10 dB of gain. This filter then removes the twin tone high frequency signal and leaves only the difference frequency signal for analysis.

5.6.8 IMD RECOVERED FREQUENCY

Frequency display in the 5500 normally shows the frequency of an incoming signal. In the IMD mode, where two mixed tones are used, frequency separation circuits are used in order to obtain a meaningful frequency display.

In the SMPTE IM mode, input signal is passed through a 3 pole 1 kHz low pass filter to remove its high frequency component allowing the resultant low frequency to be measured. The HF component is available as an output of the 2 kHz high Pass Filter.

In the CCIF mode, both the twin-tone mean frequency and difference frequency must be measured. The mean frequency is approximated by using a log compression amplifier to amplify the dead zone near zero crossing. Because near complete carrier suppression exists, this recovered mean frequency can only be measured to within a few percent. The difference frequency is recovered by first taking the absolute value of the composite twin-tone signal. A low pass filter will then remove the high frequency signal and leave only a low frequency envelope. As full wave detection is used, the frequency of this envelope is actually twice the difference frequency. This is then level shifted to a CMOS flip-flop configured as a divide by 2 circuit. The output square wave is low pass filtered to slow down the fast rising edges and minimize interference to other circuits.

5.6.9 LOGIC INTERFACE

All IM functions are controlled by the host CPU through the digital interface resident on the board. The interface circuit design follows the PROMAG™ digital interface standards. Address and data descriptions are in hexadecimal notation.

5.6.10 ADDRESS DECODING

With reference to Schematic #6b, address decoding is by U6002 (74LS85, 4-bit magnitude comparator) and by U6004 (74LS138, 1-of-8 decoder). Using links CL2 and CL4, U6004 decodes the address block between D0 and D7. U6004's outputs for addresses D0 and D1, during write cycles, are the only addresses used for all functions.

The data bus is routed to U6005 (74LS273, octal D flip-flop) and to U6006 (74LS174, hex D flip-flop); only data bits D0 - D5 are used with U6006. Both ICs' master reset control is connected to the QUIET STATIC BUS's reset control to ensure the flip-flops are in a known state after power-up.

5.6.11 IMD CONTROL

U6005, addressed at D0, has different functions under control by different groups of data bits. Data D1, D2 and D3 are used as a binary code to select eight LF oscillator frequencies. Data D4 and D5 go to U6003 (74LS139, dual 1-of-4 decoder). The binary coded data of D4 and D5 select, through U6003, one of four IM HF gain settings in the analog section. Data D6 is routed to U6001 (ULN2003, darlington transistor array). It goes to two of the transistor circuits at pin 1 and pin 5. The output at pin 16 is used as a relay driver and the output at pin 12 with the pull-up resistor is used as a logic level control. Data D7 in similar fashion connects to pins 2 and 3 of U6001. The output at pin 15 is used as a relay drive and the output at pin 14 with the pull-up is a logic level control. At the same time pin 14 goes to pin 4 whose output, pin

13 with its pull-up resistor, is an inverted logic control.

U6006, which is addressed at D1, has 3 bits used as controls. Data D0 and D1 are used as binary code for selection of 1-of-4 IMD ratios. Data bit D2 controls circuitry for selection of the sync send signals.

5.7.0 PROGRAMMABLE GAIN B (PGB)

5.7.1 GENERAL DESCRIPTION

This module is a wide band gain stage used to amplify low level signals (preamp output in wide band level mode, band pass, low pass or high pass in Narrow Band modes, notch filter out in distortion mode or IMD detector out in IMD mode). This circuit and its companion weighting filters are constructed on a plug-in PROMAG™ circuit board labelled (7) PGB/MUX.

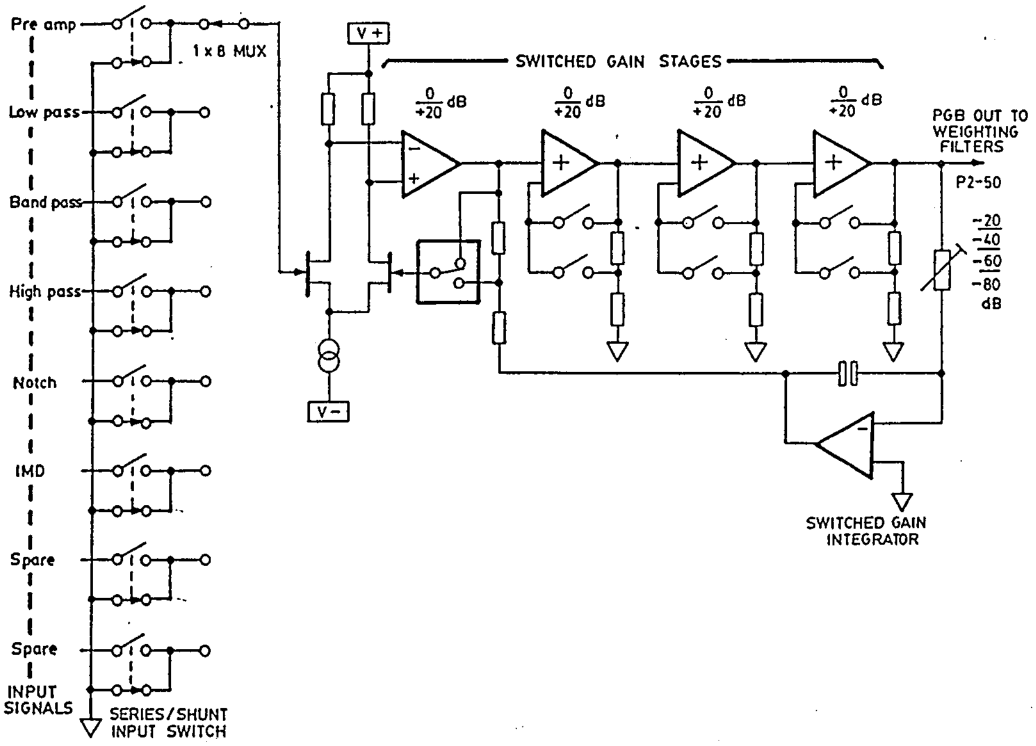

Fig. 5.7 MUX/PGB/Switched integrator simplified

5.7.2 INPUT MULTIPLEXER

PGB input is selectable from 1 of 8 sources. CMOS switches are used in a "T" (series/shunt/series) configuration to minimize crosstalk.

5.7.3 PGB

The programmable gain stages can be divided into 5 circuits: 4 x 20 dB gain stages in cascade and an overall DC feedback switched integrator. The first 20 dB gain stage, identified as +20 dB A, is a FET buffered operational amplifier and has low bias current. Its input is AC coupled and has an input impedance of 2.2 MΩ . Input FETs are biased at 2 mA with an active current source which feeds the second stage of U7003; its own front end is shut down. Gain is selected by U-7004A CMOS switches. The following gain stages labelled +20B, +20C, and +20D are identical using MA332 operational amplifiers which are high F_t and unity gain stable.

The total cascaded gain is non-inverting and is selected in the order of +20A, +20B, +20C and +20D so switching transient propagation is minimized.

5.7.4 SWITCHED INTEGRATOR

Because the 80 dB cascaded gain stages are DC coupled, millivolts of input offset could saturate the gain chain. Therefore an integrator with switchable gain is provided for offset correction. Unity and +20 dB of PGB gain sets the first step of integrator gain and each addition of 20 dB PGB gain corresponds to 20 dB of gain reduction in the integrator.

Table 5-4

	INDIVIDUAL STAGE GAIN				
TOTAL PGB GAIN	**+20A**	**+20B**	**+20C**	**+20D**	**DC INTEGRATOR GAIN**
0dB	0dB	0dB	0dB	0dB	-20dB
+20dB	+20dB	0dB	0dB	0dB	-20dB
+40dB	+20dB	+20dB	0dB	0dB	-40dB
+60dB	+20dB	+20dB	+20dB	0dB	-60dB
+80dB	+20dB	+20dB	+20dB	+20dB	-80dB

5.7.5 WEIGHTING FILTERS

Four standard filters are provided in the weighting filter section:

1) 400 Hz High-Pass 3rd-order Butterworth. This filter is in series with any one of the remaining filters. Its input and output appear both on P2 and P3 to allow special loop through insertion between preamp out and notch filter in.

2) 30 kHz Low-Pass 3rd-order Butterworth.

3) 80 kHz Low-Pass 3rd-order Butterworth.

4) "A" weighting filter or optionally, CCIR or Psophometric.

Filters 2, 3 and 4 are selected by a DG508 MUX using its first four inputs. The other four inputs appear on P3 to allow expansion of the filters.

5.7.6 LOGIC INTERFACE

The PGB board's analog circuitry is divided into three sections. The input multiplexer, PGB gain stages, and the weighting filter section. All functions are controlled by the host CPU through the digital interface resident on the board. The circuit design follows the PROMAG™ digital interface standards. Addresses and data descriptions are in hexadecimal notation.

5.7.7 ADDRESS DECODING

With reference to Schematic 7b, address decoding is by U7016 (74LS138, 4-bit magnitude comparator) and U7025 (74LS138, 1-of-8 decoder). Using decoding links CL0, CL2, and CL3, U7016 decodes the address block of A0 to A7. This qualifies U7025 where, in a write cycle only, decoded address A0 and A1 are used.

5.7.8 SYSTEM CONTROL

The data bus is routed (in reduced form, D0 - D5) to U7026 and U7027 (74LS174, hex D flip-flop). Address A0 clocks data into U7026. The first four bits D0 - D3 are used to control the weighting filter multiplexer. D0 - D2 are used in binary code to select 1-of-8 filters while D3 is the multiplexer enable control. D4 controls the 400 Hz HP filter enable. The logical invert of this is generated by an inverter in U7014 and is also fed to the P1 bus where it is used by the detector board.

D5 of U7026 and D0 - D2 of U7027 which are addressed at A1 control the PGB gain stages. Each control line also goes to an inverter because the gain circuitry requires each control line with its logical complement.

D3 - D5 of U7027 are used as the input selection controls. They are used in binary coded format and also routed to U7017 (74LS138) to be decoded. The logical invert of the decoded controls is also required and U7028 and U7015 are used for this.

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5.8.0 AUXILIARY WEIGHTING FILTERS (OPTION 005 or 006) (Reference : Schematic #8)

5.8.1 FEATURES

The optional auxiliary filter board may be provided in two standard versions or in a custom version. All versions are achieved using the same basic board but with different component populations. Schematic 8 shows all seven possible filters although typically only four would be provided. Note that the circuitry of the CCIR and Program filters are the same - only the component values change.

5.8.2 FILTER TYPES

AUDIO FILTER OPTION:

1) 20 Hz to 20 kHz Audio band pass filter or 22.4 Hz to 22.4 kHz Audio band pass filter
2) IEEE receiver filter with 19.0 kHz notch
3) "A" weighting filter
4) CCIR filter, 1 kHz or 2 kHz reference

TELECOMMUNICATION FILTER OPTION:

1) 2 kHz Flat filter
2) 15 kHz Flat filter
3) C message with 1010 Hz notch
4) Program filter

These filters are fed from the 400 Hz High Pass filter output of the PGB module and are selected by a 1-of-8 multiplexer, U8109.

5.8.3 LOGIC CONTROL

The AUXILIARY FILTERS board is an extension of the PGB board providing four additional weighting filters. The board has its own on-board digital interface, as per the PROMAG™ standards, which responds to the PGB addressing and data corresponding to the four auxiliary weighting filters. Address and data descriptions are in hexadecimal notation.

5.8.4 ADDRESS DECODING

U8003 (74LS85) and U8004 (74LS138) provide decoding with the decoded address "A0" output of U8004 controlling U8005 (74LS174). This latches data from the QUIET STATIC BUS as required for filter selection. U8005's master reset line is connected to the system reset on the P1 bus to clear the D flip-flop at power-on.

The digital control of 3 binary coded bits plus an enable bit go to a CMOS multiplexer which is identical and in-parallel to one on the PGB board. The filter mux on the PGB has filter inputs for the first four positions, the mux on the auxiliary filter board has filters connected to the last four positions. Therefore the outputs of the two multiplexers which are wired together form an eight filter selector.

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5.9.0 5500 POWER AMP EXPANSION BOARD (B-OUTPUT) (Option 007)

The B-output board option provides the 5500 system with a second signal source output. The output level and impedance will be identical as the A-output with the additional feature of being able to reverse its phase relative to A-output. The circuit board is labelled (9) B-OUTPUT and follows the PROMAG™ format. Refer to Schematic #9.

5.9.1 SIGNAL PATH

Input to the B-output attenuator is taken from the pre-attenuator signal of the power amp board.

The B-output attenuator and output impedance circuit is identical to the Power Amp and its circuit description and gain chart is valid for B-output.

B-output's independent phase and output "ON" switching is by a two Form-C relay in the signal path before the output attenuator. A metal shield box provides the floating and shielded isolation similar to that on the main power amplifier.

5.9.2 CONTROL LOGIC

The B-output's control logic codes are identical to the power amp's for output attenuation and impedance. Additional codes provide control over the independent functions. B-output has its digital interface circuitry resident on the board and the circuit design follows the PROMAG™ digital interface standards. Address and data descriptions are in hexadecimal notation.

5.9.3 LOGIC INTERFACE

The additional logic codes required are latched in a 74LS174 Hex D- Flip-Flop address at C3 and drive relays through U5907 (ULN2003).

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5.11.0 POWER SUPPLY SUBSECTIONS OVERVIEW

Ref: Schematic #11A & 11B
Simplified Block Diagram Figure 5-9

The 5500 Power Supply module provides several regulated and monitored supply rails. Each rail contains short circuit protection, over and under voltage monitoring and overcurrent protection.

The power transformer is of toroidal construction to reduce radiated interference. Several primary taps are provided to permit operation from any common international mains supplies.

Heat sink mounting is included for high power rails and forced air cooling ensures proper thermal management.

The following supply rails are provided:

+5 V 5 A CPU and logic
± 12 V power supply
± 12 V 250 mA Serial communication
± 19 V 2 A Analog pre-regulated rails
± 35 V 400 mA Isolated power amplifier

5.11.0.1 5 VOLT SUPPLY

This section supplies the voltage requirements of the 5500 CPU board and the digital interfacing logic resident on each PROMAG™ board. The circuit is implemented by a Unitrode UC3834 voltage regulator with crowbar over-voltage protection.

5.11.0.2 V-STBY GENERATOR

Provides the supply voltage requirements of the non-volatile memory located on the CPU board. The V-STBY generator is not switched by the 5500 power-on button but remains operational unless the 5500 is not connected to AC mains. It also has the function of trickle charging three NICAD batteries which automatically provide V-STBY to the non- volatile memory when no AC mains is connected.

5.11.0.3 ± 12 VOLT UNSWITCHED SUPPLY

This section provides the bi-polar voltage requirements of the power supply control circuitry. This section remains powered as long as AC mains remains connected and is implemented by low power 3-terminal regulators.

5.11.0.4 ± 12 VOLT SUPPLY

This section provides the bi-polar voltage requirements for the two RS232 communication ports that can be installed. The circuit is implemented by two Unitrode UC3834 voltage regulators with crowbar over-voltage protection.

5.11.0.5 ± 19 VOLT SUPPLY

This section provides the bi-polar voltage requirements for the analog circuitry resident on each PROMAG™ board in the 5500 system. Each PROMAG™ board provides post regulation to ± 15V using three terminal regulators. This method has the benefit of reducing power dissipation both in the supply and on each PROMAG™ board while also providing greater isolation between boards.

5.11.0.6 ±35 VOLT SUPPLY

This section provides the bi-polar requirements of the output section of the Power Amp board. The circuit is designed so that the Unitrode UC3834 voltage regulators can operate properly in a requirement that normally would exceed their maximum input supply rating.

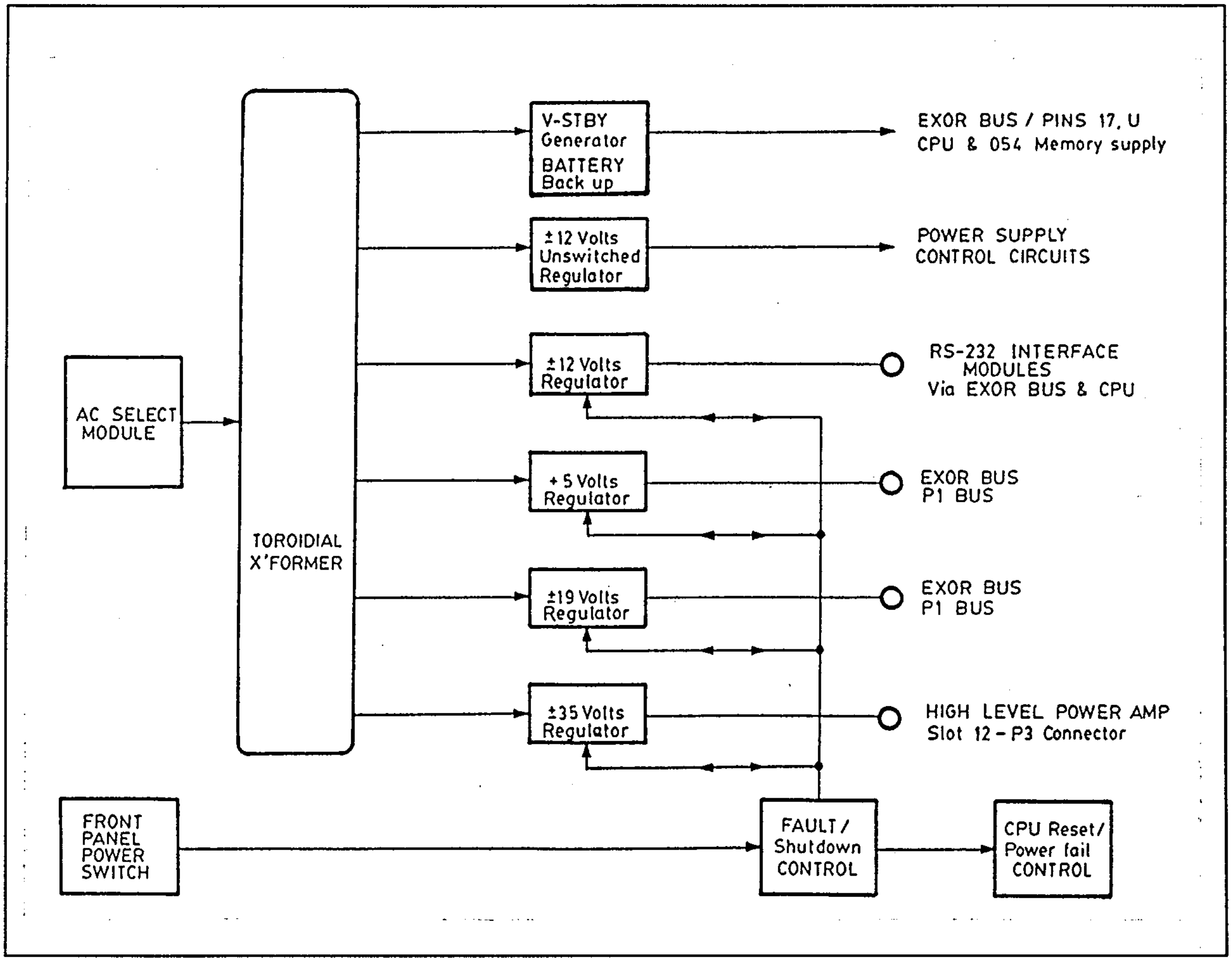

Fig. 5.11 Power supply and control simplified

5.11.1 POWER SUPPLY CONTROL CIRCUITRY

The power supply system control circuitry is designed to be able to shut the complete supply off when any subsection sends a fault condition signal on a common wired-OR input. Details of controlling the subsection's regulators and their implementation is described in a later section.

The 5500 system power switch is a special case of the fault/shutdown circuitry. The power supply's AC and pre-regulated DC circuits are not switched but remain active if AC mains is connected.

The control circuit operation can best be described starting with the system being in the "ON" state with no subsystem faults.

The power-on front panel switch being closed keeps Q8034 (IVN5001AND - MOSFET) in a non-conducting condition. Through pull-up resistors the common FAULT line is kept high and through R8063 this level is connected to the negative input of a comparator (U8006, pin 10). This is a higher voltage than V-ref (generated by Q8022, TL431) at the positive input, causing the output to be at circuit common level. This is fed to the negative input of another comparator (U8006, pin 6) whose positive input has a voltage level set by a divider network. This causes the output (U8006, pin 1) to be at a high level by a 4k7 pull-up. This output called SHUTDOWN is the control input to the UC3834 regulators where a high level is normal operation.

With the power-on switch open (system OFF) or, if a subsection pulls the fault line low, the comparator output (U8006, pin 13) will go high. But since the comparator is an open collector type, the output will go high at a rate set by the time constant formed by R8059 and C8029. This allows a delay before the second comparator pulls the SHUTDOWN signal low. This delay of approximately 1/4 second allows any transient fault conditions to pass without shutting down the system.

5.11.2 VOLTAGE REGULATION

As previously mentioned, the main voltage regulator used in most of the power supply subsystems is the Unitrode UC3834 linear regulator. Its main features are a low input/output differential voltage, usable for positive or negative supplies, adjustable current sense, and over/under voltage alerts with programmable delay.

Using the Unitrode data sheet and the positive 19 Volt subsection schematic for reference, the general implementation can be described.

Q8031 is used as the external pass device with the driver sink current control from pin 12. Pin 9 is one input of the regulator error amp which senses the output voltage through the divider network formed by R8089 and R8088. The other error amp input is pin 8 which is connected to an internal reference voltage generator at pin 3.

The resistor network formed by R8100, R8101, and R8102 provides the current sense amp at pin 6 and 7 a voltage representation of the output current. The resistors are chosen to program the maximum output current required under worst case conditions for each subsection.

The internal fault monitoring circuit, after a programmed delay set by C8046 connected to pin 11, will provide a fault alert output on pin 10. This is connected to the common fault line of the control circuit.

The SHUTDOWN control is connected back to the UC3834 through a comparator IC to pins 14 and 15. Any fault in the system causes SHUTDOWN to go low and turn each subsection off.

The negative rail implementation is quite similar except for a few simple additions.

The internal reference voltage is a negative source at pin 2 connected to pin 9 of the error amp and both the fault output and the shutdown control input use extra circuitry to level shift the controls.

LEDs connected to both rails provide a visual indication of voltage being present. These LEDs, as on the other subsystems, are mounted on the PCB. A problem on a subsystem may be spotted because a LED will not light during the 1/4 second fault delay interval before system shutdown.

5.11.3 REGULATOR MODIFICATIONS

There are special additions to the UC3834 subsections to provide extra functions.

On the ± 19 Volt subsection, TRANSORBS are installed across the filter caps. The transformer windings for this section have a very large VA capacity. If a large mains over-voltage condition exists, these transorbs will short causing a large mains current and blow the AC mains fuse. The system will require repair but catastrophic damage will have been prevented.

The ± 12 Volt and the 5 V subsections utilize the crowbar output of the Unitrode UC3834 regulator. This control output is activated following a sustained over-voltage condition such as if the pass transistor shorted out.

Using the 5 Volt regulator as an example, Q8028 (TIC126, SCR) is installed across the output rails. In an over-voltage condition, the crowbar output at pin 16 will turn on the SCR. This accomplishes two things. First, the large current flow because of the SCR shorting the output will blow the fuse in series before the pass transistor. Second, the now shorted output will force the UC3834 into a fault condition which will shutdown the 5500 supply. As with the transorbs, damage will be limited if a fault develops.

The ± 35 Volt subsection required additional circuitry to allow the Unitrode UC3834 regulators to be used where the unregulated DC voltage exceeds the maximum input supply voltage rating of the chip.

Using the +35 Volt circuit as an example, D8007, a 15 Volt zener diode, drops the supply voltage to the UC3834. And D8010 performs the level shifting required for the pass transistor driver output. Over- current sensing is level shifted by the circuit made up by Q8010, R8020, R8024 and R8021. The voltage across R8021 will reflect the output current.

An additional requirement of the ± 35 Volt supply is that it be floating with respect to all other supply voltages. This requires a method of isolating the fault alert outputs and the input shutdown controls. Opto-isolators U8008, U8009 and U8010 interface the system control circuitry.

The two transformer windings that supply the ± 35 Volt supply have an additional electrostatic shield which is connected to ± 35 Volt supply common. This serves to shield these two windings from the other primary and secondary windings.

5.11.4 CONTROL CIRCUITRY

Support control circuitry for the CPU board is installed on the power supply board. It provides the CPU with an indication of a stable power rail with an early indication of a failing supply, and the power-on reset control. Additionally, the 5 Volt supply is adjustable as is the V-stby generator which supplies the non-volatile memory supply.

The power fail circuit is designed to give the CPU an early indication of a problem so that the programming has the chance to store the 5500 operating state for later recall.

Two comparators in the U8005 package (output pins 2 and 1) along with Q8016 form the multifunction sense circuit.

Comparator input pin 5 will sense a power supply system fault or the front panel switch going to the OFF position. Comparator input pin 6 will sense the failure of AC power or low line condition.

The CPU reset control signal is generated by two comparators (output pins 13 and 14 of U8005) with their associated circuitry. When the power supply is turned on, U8005 pin 13 switches low (comparators negative supply). This shuts off Q8019 allowing C8028 to charge through R8051. This RC sets the delay time for the reset control after power-up allowing the 5 Volt supply time to stabilize before the CPU is allowed to begin operating.

An external connection has been allowed for at this point for an external reset control by shorting C8028 to 5 Volt common.

The voltage on C8028 will switch U8005 pin 14 low. This switches U8018 off and the reset control line is pulled to nearly 5 Volts by R8053 and Q8017 with the associated circuitry.

The 5 Volt supply is the only major section with allowance for adjusting the output voltage. Trimpot VR8002 allows adjustment from 4.8 to 5.3 Volts. This is set to 5.10 Volts measured on the power supply output connector.

The V-stby generator provides the supply voltage to the non-volatile memory resident on the CPU board and also keeps the NICAD batteries charged. This circuit is not switched and remains operational as long as the unit is connected to mains. When not connected to an AC source, the NICAD batteries maintain the supply voltage to the memory.

Input to the LM317 adjustable regulator (Q8027) is from a high unregulated DC voltage to provide operation even under low line conditions. VR8001 with associated components provide adjustment of the output voltage. Q8025 is implemented as a base-collector forward biased diode which, when the regulator is not operating, provides a low leakage blocking diode from the battery circuit. Q8026 with its associated circuitry provides a dynamic load to the LM317. This is done because the very low current requirements of the memory, especially when the 5500 is off, would not be enough to ensure regulation. R8069 provides the battery charging rate and, again because of the memory's low current needs, causes minor voltage loss when the 5500 is disconnected from mains.

5.11.5 AC MAINS

The AC circuit is comprised of the transformer along with the mains voltage selection switching and the switched fan used for internal cooling.

Input AC voltage selection is provided for by a combination connector/tap selector/fuse/filter. The voltage select drum along with the four transformer primary windings provide nominal AC voltage selection of 100 V, 120 V, 220 V, and 240 V.

The transformer secondaries are rated to provide approximately 300 VA of rated secondary current. As the system is designed to operate at 50 Hz and there are temperature rise limitations, the toroid transformer uses a 500 VA core. An electrostatic shield is provided to isolate primary and secondary windings.

The 5500 fan, used to cool the power supply pass transistor heatsink assembly and to maintain an even heat distribution throughout the internal area of the 5500, is powered from a 100 V AC secondary winding. It is switched by a solid state relay controlled by the 5 Volt supply.

5.11.6.0 TYPICAL PERFORMANCE SPECIFICATIONS

5.11.6.1 5 VOLT SUPPLY

Output ripple and noise at rated current and 10% low AC line: less than 5 mV (0.1%) typical.

Output impedance at midband frequencies: less than 0.2 ohm typical.

5.11.6.2 ± 12 VOLT SUPPLY

Output ripple and noise at rated current and 10% low AC line: less than 6 mV (0.05%) typical.

Output impedance at midband frequencies: less than 0.5 ohm typical.

5.11.6.3 ± 19 VOLT SUPPLY

Output ripple and noise at rated current and 10% low AC line: less than 20 mV (0.1%) typical.

Output impedance at midband frequencies: less than 0.6 ohm typical.

5.11.6.4 ± 35 VOLT SUPPLY

Output ripple and noise at rated current and 10% low AC line: less than 30 mV (0.1%) typical.

Output impedance at midband frequencies: less than 3 ohms typical.

5.12.0 CPU BOARD FUNCTIONAL DESCRIPTION

The CPU board (Drawing #12 - CPU) serves a number of functions in the PROMAG™ system. Not only does it contain the microprocessor and its support logic, but it also supports a total of five distinct communications channels to allow it to be controlled by or to control other systems or subsystems. In addition, it provides the digital support logic for the system's data acquisition.

5.12.1 PHYSICAL & ELECTRICAL CHARACTERISTICS

The board is designed to conform closely with the physical and electrical characteristics of Motorola's Exorbus. In the active mode, the board draws approximately 750 ma from the 5 volt logic supply and 100 ma from the 5 volt standby logic supply. In the quiescent state the board draws only a few microamps from the standby supply to retain the contents of its non-volatile RAM. For systems not providing a standby supply, provision is made to install a lithium type primary cell on-board for memory retention through power down. The 5 volt logic rails are provided with transient voltage and supply reversal protection while diode D6 guarantees that the logic supply cannot exceed Vstandby by more than 0.6 volts. Extensive power supply decoupling is provided by a combination of distributed capacitance bus bars, ceramic decoupling caps and large value bulk electrolytic.

5.12.2 MICROPROCESSOR

The MPU used is a 6809 type processor provided with an internal clock oscillator which is disabled and driven by the main system timebase as described below. The design of the MPU support logic is such that it is possible to use this MPU as the main Exorbus system processor, or to remove the MPU from its socket and treat the CPU board as a peripheral board to another MPU.

5.12.3 SYSTEM TIMING LOGIC

The low drift 8 MHz oscillator U1 provides the signal from which two important timebases for the system are derived. The MPU clock may be taken directly from U1 or may be divided by U2 to provide operation at 0.5 or 1 usec cycle time, respectively. U2 is also used to provide the 2 MHz REF clock used by various system timers for delay measurements and data acquisition. A programmable delay circuit is implemented using U25 and its associated gates to provide a means for MRDY stretching the MPU E clock during Static Bus accesses, allowing relaxed timing requirements for Static Bus devices. Note that E is not used for any real time measurements.

5.12.4 ADDRESS DECODING LOGIC

A bipolar prom, U28, provides the highest level of address decoding for the system, producing a four bit output code as a function of the address bus which is connected to its eight lowest address inputs, giving a decoding resolution of 256 locations. The highest address input to U28 is available for use in map switching in a debugger environment and all the outputs are qualified by a signal that can be derived from Exorbus signals VXA, VUA or VMA. The three lowest order outputs of U28 provide the select inputs for one of eight decoder U20 which directly drives the active low chip select inputs of the five available memory sockets, U3, U8, U13, U21 and U29. The MPU bus peripherals and the PROMAG™ Static Bus are enabled by two of the remaining outputs. The outputs of U20 are further qualified by RESET and a locally generated signal VMA*. Another one of eight decoder, U16, is qualified by U20 and decodes A4 to A6 to give a decoding resolution for the MPU bus peripherals of 16 locations.

5.12.5 MEMORY SUPPORT LOGIC

The five memory sockets can be configured in a number of ways to support virtually any useful combination of JEDEC pinout ROM and RAM. One device, U29, is expected to be an 8K to 32K EPROM or ROM type device, while U21 and U13 may be configured as 8K to 16K EPROMs or ROMs or 8K RAMs. U8 and U3 may be configured as 8K to 16K EPROMs or ROM or as 2K or 8K RAMs. Standby power is provided on U3 and optionally on U8 and U13 when these devices are specified as non- volatile RAMs. Two gates of U19 provide read and write signals qualified by E for driving the WE* and RE* inputs to the memory devices. When U3 is an 8K RAM device, pin 26(CS) is brought to the unbuffered Exorbus RESET signal through a current limiting resistor R4 to guarantee the integrity of the RAM data through power fail. A high impedance pull down resistor, R3, provides a low logic level on this pin if the board is removed from the Exorbus connector. See below for the requirements of the off board reset generator.

5.12.6 EXORBUS SUPPORT LOGIC

The CPU board interfaces to the Motorola Exorbus via P5. Comprehensive support for operation with other Exorbus boards is provided and allowance made for the data acquisition board to be either an Exor master or slave. Several unique signals not normally provided on the bus can be disabled for operation with other boards which may themselves make use of these unassigned pins. The two most of concern are EXVMA* on pin H of the bus, which can be used to qualify DMA transfers and the SYNC instruction, and EXHF on pin 26 which can be used as an accurate timebase for other subsystems on the bus. The EXVMA* signal is derived from the on-board VMA produced by clocking the state of BA on the falling edge of E. This provides a necessary qualifying signal to be used with DMA, HALT or the SYNCH instruction.

The direction of the Exorbus data buffer is controlled by a signal produced by the highest output line of address decoder PROM U28, which provides a logic low level whenever an on-board device is decoded. This signal may be modified by the BA line going high, indicating that either a DMA transfer is in progress or that U12 (the MPU) is not present.

No provision is made on-board for reset generation as this is a complex function that is expected to be handled by the power supply. It is required that the Exorbus RESET line be taken to a logic low level before the power supply has fallen below that required for proper functioning of the logic circuits and that it not be allowed to rise to a logic high level until at least 200 msecs after the power supply has risen to a valid level. In addition, the level present on the Exorbus RESET line should be maintained at a value between -0.1 volt and 0.3 volts while the system is in its standby state to minimize power consumption from the standby supply or the on-board battery. If these requirements are met, the validity of the data in the RAM can be guaranteed through power fail. An input is provided on U11 to receive a "impending power fail" signal from the Exorbus power supply and this signal may be connected to NMI to asynchronously alert the processor.

5.12.7 STATIC BUS CONTROL LOGIC

The PROMAG™ system uses a relatively straightforward synchronous bus structure to allow the CPU to communicate with measurement hardware and certain types of front panels. The basic bus is organized as an eight bit address bus and an eight bit data bus, with signals provided that are properly timed to allow the orderly transfer of data to Static Bus data consumers and from Static Bus data producers. No provision is made to allow more than one Static Bus master on the bus.The Static Bus is accessed via P1 on the board.

The CPU board treats the devices on the Static Bus as memory mapped peripherals and allows both the writing of data to peripherals and the reading of data from them. Attempts to write to non-existent consumers or read from non-existent producers will not cause any bus contention. U14 is used to buffer the address lines from the MPU to the Static Bus and because the Static Bus is memory mapped, it merely latches the lowest eight bits of the MPU address bus at the start of any valid Static Bus transfer. The outputs of U14 are always enabled, imposing the restriction of a single Static Bus master. The data presented by the MPU on a Static Bus write cycle is clocked into U9 after the data bus has stabilized, providing latched data to be taken by any Static Bus data consumers, while U4 is used as an input buffer to allow the MPU to read any data presented by an Static Bus data producer. The direction of data traffic on the bus is determined by the SBRD line which is derived by latching the state of the MPU R/W* line during Static Bus accesses using gates from U19 and U22.

A critical timing signal named SBODV* is generated on the falling edge of Q during valid Static Bus transfer cycles and remains in its active low state until the falling edge of E. As mentioned above, the Static Bus transfer timing is stretched by U25 and its associated gates, giving a worst case address or SBRD to SBODV fall of 125 nsec and 500 nsec data valid to SBODV rise specification. It is expected that Static Bus data consumers will transfer data on the low level of SBODV or on its rising edge. Data, address and SBRD hold times are in excess of 250 nsec, as they are latched until the start of the next valid Static Bus transfer. Static Bus data producers are expected to have an address access time of less than 500 nsec and a chip select access time of less than 350 nsec.

5.12.8 DATA ACQUISITION LOGIC

Hardware is provided to count the negative transitions of two signals that are presented by the Static Bus and to simultaneously count transitions of the REF signal generated by U2. This may be used to measure the frequencies of the signals which are typically used to represent the frequency and amplitude of some test signal. Gating logic is provided by a flip-flop in U18 with gates from U15 to allow the accumulation of counts to be synchronized to one of the two signals. This is extremely useful for the classical "frequency measurement by period inversion" technique and provides the necessary synchronizing signal for the synchronous integration method of amplitude measurement when one of the signals represents the output of a voltage to frequency converter.

A total of six counters, provided by U5 and U10, are available in the system. One of the counters in U5 can be used by the executive software as a real time clock or as a tick generator for time slicing. The remaining two counters of U5, pre-scaled by the two four bit counters of U17, are used in conjunction with one counter of U10 to form the synchronously gated counter set. The remaining two counters of U10 are available as software gated counters for counting the reference clock and one of the two inputs. The prescale counters in U17 may be read by U11 and may be reset by its CA2 output.

5.12.9 ASYNCHRONOUS SERIAL COMMUNICATIONS

Comprehensive support for two async serial ports is provided by U6 with baud rate generator crystal X2. The 2681 device provides flexible control of such parameters as baud rate, stop bits and handshaking. No buffers are provided on-board to interface to the transmission medium, although standard accessory boards can provide RS 232 interfaces via connectors P2 and P3. Five volt logic supply and bipolar twelve volt communications power are brought to these connectors from the Exorbus interface, with the twelve volt supplies diode isolated as per manufacturers' recommendations for EIA drivers.

5.12.10 IEEE 488 (GPIB) INTERFACE

Hardware is provided to interface the board to the GPIB via U7. The 68488 device provides talker and listener capability for the system. Bus drivers are not provided onboard but are supplied on a standard accessory board. Five volt logic power to drive the buffers is supplied to the interface connector P4 from the Exorbus logic supply.

5.13.0 5500 KEYBOARD AND DISPLAY BOARD

Ref: 5500 Keyboard and display Schematic #13

The keyboard and display board provides the primary mode of interfacing between an operator and the instrument. GPIB and RS232 communication ports provide alternate modes of control.

The PCB is comprised of all push buttons required to operate the 5500, all seven segment displays and LED tallies for instrument readings and status information and all the digital hardware to provide bi-directional interfacing to the 5500 CPU controller. Communication to the CPU is via a 50-wire ribbon cable connected to the CPU's "STATIC BUS" which is the first of two levels of the buffered parallel port used by the CPU to communicate with subsystems within the instrument. Only the "Power ON" button is directly wired to the hardware based power supply control circuitry using a four-pin Molex connector.

A second 4-pin connector provides +5V and GND in addition to power being present on the ribbon cable. This provides all power for the logic circuits and displays except for the button scanning circuit which requires a -12V source. This is derived from -19V available on the 50 wire ribbon.

5.13.1 ADDRESS DECODING

Address decoding is by a bi-polar PROM (U901) and a dual 1-of-4 decoder (U902) which provide device selection of all sections on the board. The 3 LSB address lines (A0 - A2) are buffered from the static bus (U904) because of the multipoint routing and CMOS level pull-ups required.

Three ICM7218E CMOS universal 8 digit LED driver chips are used for all display functions (U901, U911, U912). They each have on chip an 8k x 8 static memory array providing storage for each segment and LED in the output matrix. The host CPU needs only to write data via the 8 bit data bus to the memory locations corresponding to the displays being turned on or off. The chip independently maintains its multiplex scan circuitry and has on-board all the required high power digit and segment drivers. All three ICM7218 chips are used in the NO DECODE mode which means that input data is not in a coded format. In addition, the shutdown control (pin 10) of each ICM7218 is connected to the STATIC BUS RESET signal so that all displays are off when the host CPU is in its initialization mode during the first few seconds of instrument turn on. This prevents the random data that would be displayed before the host CPU has had time to set up displayed information.

5.13.2 KEYBOARD ENCODING

The front panel buttons are scanned by the KR-9600 PRO keyboard encoder IC (U908). It contains a 3600 bit read only memory and all the logic necessary to encode SPST keyboard closures into a 10 bit code with switch debouncing.

When a key is depressed, a signal pulse from the DATA READY output (pin 16) sets the SERVRQ* (service request) line on the STATIC BUS through latches U905 and gate U903B. The host CPU in the process of reading the ANY KEY OUTPUT line (pin 5) buffered by U904, will reset the SERVRQ latch for the next switch closure. The host CPU then reads the encoded data through the data bus buffer (U907).

The SHIFT key is debounced by U920A and B and latched by U921A. If U921A is set (i.e. SHIFT is active) when a key is pressed, it is reset by U921B clocked by the DATA READY output of U908.

5.14 5500 GPIB INTERFACE
Ref: Schematic #14

The 5500 GPIB interface board is located at the back of the unit. Through a 26-wire ribbon cable to the 5500 CPU, the board provides the interface to the IEEE Standard Instrumentation bus (488-1978).

Two MC3447 octal bi-directional bus transceiver ICs are located on the board providing direct connection to the GPIB bus. Transceiver direction is controlled by the host CPU and there are no other required components located here since the MC3447 provides the bus standard termination internally.

+5V and GND is provided through the 26-wire ribbon cable by the host CPU.

5.15.0 5500 RS232 INTERFACE BOARD
Ref: Schematic #15

The 5500 RS232 interface is located at the back of the unit and connects to the host CPU via a 24-wire ribbon cable. Located on the board is a MC1488 quad line driver and a MC1489 quad line receiver IC providing bi-directional interfacing to equipment in conformance with the specifications of EIA Standard RS-232C.

A configuration header on the board allows setting up the RS232 interface so that the host CPU may be either DCE or DTE standard.

Power to the board is provided by the host CPU and includes +5 and GND, ±12 and 12V com.